



# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

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Applicant(s)

Chen et al.

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7/18/2003

Group Art Unit

2818

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

NN		H. Akatsu et al., "A highly manufacturable 110nm DRAM technology with 8F2 vertical transistor cell for 1Gb and beyond", IEEE 2002 Symposium on VLSI Technology Digest of Technical Papers
NN		K. McStay et al., "Vertical pass transistor design for sub-100nm DRAM technologies", IEEE 2002 Symposium on VLSI Technology Digest of Technical Papers
NN		J. A. Mandelman et al., "Challenges and future directions for the scaling of dynamic random-access memory (DRAM)", IBM Journal of Research and Development, Vol. 46, No. 2/3, March/May 2002, pp. 187 - 208

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DATE CONSIDERED

10/28/2006

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